

Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 4.4pF STM8L152C6T6 [LQFP(7x7) 0.5mm pitch]

Measurement conditions : Vdd=1.8V and 3.0V at 25°C

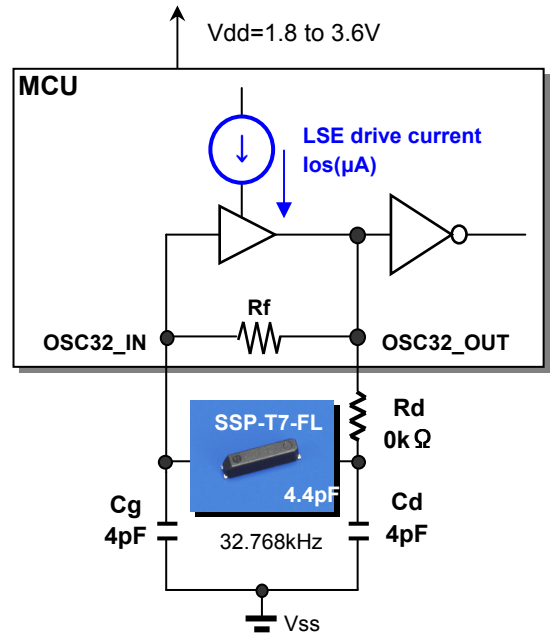
STM8L152C6T6 LSE oscillation circuit and recommended load capacitance

For STM8L152C6T6

LSE oscillation circuit consists of an excellent power saving circuit which realizes stable oscillation at low amplitude.



For your design reliability, please refer to Table 1 which shows the performance of the LSE oscillation circuit and the recommended load capacitance for each resonator.



$$C_{ext} = \frac{C_g \times C_d}{C_g + C_d}$$

$$CL = C_{ext} + C_s (=2.35pF)$$

SSP-T7 series

SSP-T7-FL CL=3.7pF, 4.4pF, 6.0pF and SSP-T7-F CL=7.0pF, 9.0pF, 12.5pF
 VT-200-FL CL=3.7pF, 4.4pF, 6.0pF and VT-200-F CL=12.5pF

Table 1 LSE and load capacitance for a resonator

XTL	CL (pF)	Rd (kΩ)	Cg (pF)	Cd (pF)	Vdd	Ios (μA)	dF/Cext ⁻¹ (x10 ⁻⁶)	Ts (sec)	RL (kΩ)
SSP-T7-FL	4.4pF	0	4	4	1.8V +10%	0.220	3.74	0.82	-728
					3.0V ±10%	0.224		0.77	-738
VT-200-FL	6.0pF	0	7	7	1.8V +10%	0.220	3.99	1.50	-397
					3.0V ±10%	0.224		1.37	-397

*JGRM1552C1HxR0CZ01D1 and GRM1554C1H2R0CZ01D(±5%).

Low power consumption STM8L152C6T6 and SSP-T7-FL

